

**PAVITHRA.S**

PCB Design Engineer

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### **Objective:**

Looking forward to work in an organization that offers challenging opportunities and which provides innovative work, growth and wide exposure to the latest technologies.

### **Profile Summary:**

- ▶ Over all 5 year experience in designing PCB boards.
- ▶ Expertise in PCB and ATE designs.
- ▶ Complete CAD design flow from Schematics, Library creation, Layout design, routing, Power plane and split power plane, non-electrical and Gerber release.
- ▶ Designed PCB boards for the automotive industry.
- ▶ Creating & checking the Gerber & Plot files.
- ▶ Have done PCB layout design which includes high speed Signals, Analog signals, digital and mixed signals boards for various applications.
- ▶ Analyzing the input data for sufficiency and validity.
- ▶ Effective communication with customers over emails to address any issues or requirements.
- ▶ Have interpersonal skills, committed, result oriented, team work, hard working with a quest and zeal to learn new technologies.

### **Educational Qualifications:**

B.E in ECE - Sri Ramakrishna Engineering College, Vattamalaipalaiyam, Coimbatore with CGPA 8.5

### **Professional Experience:**

- ▶ Valeo India Pvt Ltd, Chennai – Jul 2019 to Aug 2020
- ▶ Caliber Interconnect Solution Pvt Ltd, Coimbatore – Sep 2015 to Jul 2019

### **Technical Experience:**

- ▶ Handled up to 60 Layer PCBs Containing BGAs, PGAs, fine pitch SMD and through hole Components using technologies such as Differential pair routing, Strip plane, Microstrip, Propagation delay matching, Guard banding, Grid based routing.
- ▶ Worked in High speed interfaces such as USB, Ethernet.
- ▶ Experience as a Front End Engineer for 70+ ATE layout designs.
- ▶ Finest device pitch handled: 0.35mm, 0.4mm and 0.5mm.
- ▶ Good knowledge in Micro/Laser, blind and buried Vias.

- ▶ Good knowledge in impedance calculations and effective design of multiple impedance traces over the same layer in multiple design configurations.
- ▶ Adequate knowledge on DFM and DFA to ensure successful & cost effective manufacturing/assembly in design stage itself.
- ▶ Ability to optimize the design for signal and power integrity based on the SI engineer guidance.
- ▶ Experienced in handling Motherboard, daughter cards and Flex board designs.

**EDA tools:**

- ✓ Orcad Capture
- ✓ Concept HDL
- ✓ Cadence Allegro 15.7, 16.x and 17.2
- ✓ Polar SI
- ✓ CAM350, View mate (basic & IPC net list checking)

**Projects:**

**1. Smart Bar Door Design:**

<b>Scope of work</b>	Design Engineer & Layout to Gerber's
<b>Tool</b>	Cadence Allegro
<b>Min Pin Pitch &amp; Board Thickness</b>	0.5 MM & 1.6 MM
<b>No. of layers</b>	6 Layers
<b>Total no. of components and Nets</b>	453 & 250

**Major components & Highlights:**

- Constraint setting and routing. For fan-out used laser via, buried via.
- Buck converter & microcontroller placement and touch signal routing done in outer layer.
- All impedance signals routed in single layer and Ground splitting.

**2. High Speed:**

<b>Scope of work</b>	Design Engineer & Layout to Gerber's
<b>Tool</b>	Cadence Allegro
<b>Min Pin Pitch &amp; Board Thickness</b>	1 MM & 6.8 MM
<b>No. of layers</b>	42 Layers
<b>Total no. of components and Nets</b>	2247 & 2465

**Major components & Highlights:**

- Maximum Speed of the TX/RX signal is 25GHZ (Loopback)
- Performed High dense placement to achieve 4 inch length for TX/RX

- Hybrid Stack up with Low dielectric constant material for High speed signals
- Critical to achieve the high speed signal routing in minimum layers with 4 inch length
- Back drill has been done for all the high speed signals

### 3. RF based transmission

<b>Scope of work</b>	Design Engineer & Layout to Gerber's
<b>Tool</b>	Cadence Allegro
<b>Min Pin Pitch &amp; Board Thickness</b>	1 MM & 3 MM
<b>No. of layers</b>	22 Layers
<b>Total no. of components and Nets</b>	248 & 365

#### Major components & Highlights:

- Schematic Creation (Orcad) & Component placement with mechanical housing restriction .
- Placement and routing was done with Analog and digital signal consideration, SMA connectors were placed as much close to the RF nets.
- RF routing is critical on outer layer, so this is achieved by adding stitching via.
- Implemented SI specifications for the high speed 2.4Gbps signal routing.
- Constraint setting and Routing.
- Stitching via's placement and back drilling done for high speed Signals.

### 4. DIGIWAVE:

<b>Scope of work</b>	Design Engineer & Layout to Gerber's
<b>Tool</b>	Cadence Allegro
<b>Min Pin Pitch &amp; Board Thickness</b>	0.8 MM & 1.6 MM
<b>No. of layers</b>	10 Layers
<b>Total no. of components and Nets</b>	3508 & 2365

#### Major components & Highlights:

- Placement is critical to achieve in provided board size.
- Followed fly-by topology for DDR3 address signals.
- Constraint setting with pin pair group and delays.
- Length Matching done as per the given Specification.

**Personal Details:**

Father's Name: Karuppusamy A  
Date of Birth: 02-05-1993  
Languages Known: English, Tamil  
Hobbies: Mehandhi designing, Gardening  
Permanent address: 113, Elango Nagar, Avarampalayam  
Coimbatore- 641 006.

**Declaration:**

I hereby declare that all the information mentioned above is true to the best of my knowledge

Place:

Date:

Yours sincerely,

Pavithra.S